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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/993,094	11/06/2001	Shigeo Matsumoto	SONYJP 3.0-217	6045

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EXAMINER	
VU, PHUONG T	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 06/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/993,094	MATSUMOTO ET AL.	
	Examiner	Art Unit	
	Phuong T. Vu	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klatt et al. (US 6,097,605) in view of Oliphant et al. (US 6,461,170B1). Regarding claim 1, Klatt discloses an integrated circuit device adapted to be loaded in host equipment comprising a substantially rectangular main body unit 5, a first set of connection terminals 7 provided at one end of said main body unit to enable electrical connection between said main body unit and the host equipment, a plurality of loading sections 21, 22 provided in said main body unit, each of said loading sections having an insertion opening along an edge of said main body unit transverse to said one end, a second set of connection terminals (necessarily provided for interfacing with inserted multimedia card MM) spaced from said insertion opening, and a pair of sidewalls (walls directly adjacent loading sections 21, 22) disposed between said insertion opening and said second set of connection terminals, a plurality of substantially rectangular integrated circuit chips MM assembled in respective ones of said loading sections, each of said integrated circuit chips including a built-in integrated circuit unit forming a memory unit or a logic circuit and a third set of connection terminals (contacts provided on the

multimedia cards MM) for establishing electrical connection between said second set of connection terminals in said loading section and said integrated circuit unit, and a controller necessarily provided and disposed in said main body unit for controlling the writing of information signals to and the readout of information signals from said plurality of integrated circuit chips loaded in said loading sections. Klatt does not disclose a guide support provided in each of said loading sections and extending in a direction transverse to said insertion opening for guiding the insertion of said integrated circuit chips into said loading sections, each said guide support including a pair of guide recesses formed along said pair of sidewalls of said loading section. However, Oliphant teaches that it is known to provide an integrated circuit device 40 adapted to be loaded in host equipment, a loading section provided in the main body unit 42, a guide support (area opposing guide recesses) provided in each of said loading sections and extending in a direction transverse to an insertion opening for guiding the insertion of a card into said loading section, the guide support including a pair of guide recesses (notches along inner portion of sidewall of 42) formed along a pair of sidewalls (outer walls of 42)

of said loading section (see figure below).

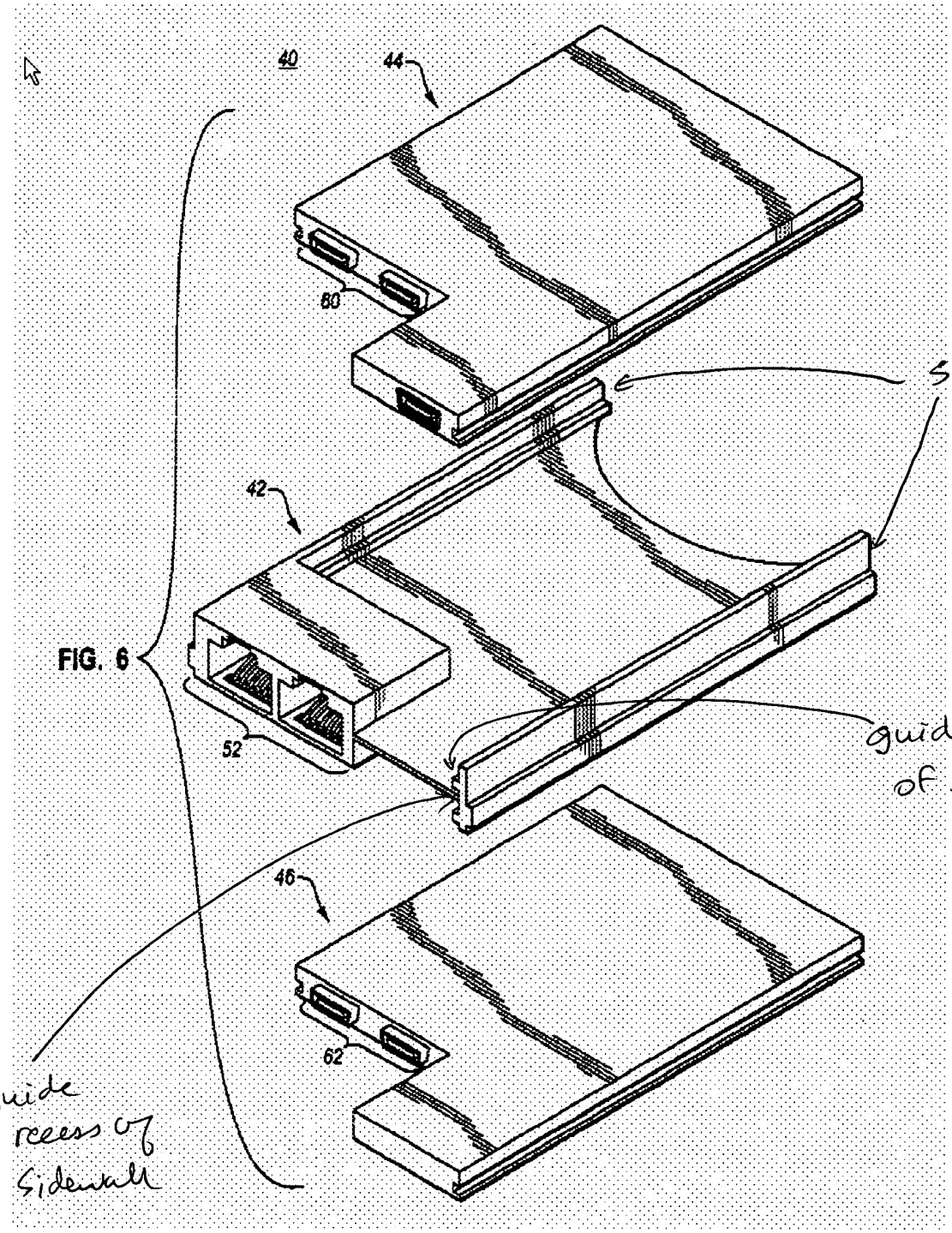

FIG. 6

The Oliphant reference is relied upon solely for the teaching of providing an integrated circuit device adapted to be loaded in host equipment wherein the integrated circuit device has loading sections provided in a main body unit, and a guide support is provided in each of said loading sections and extending in a direction transverse to an insertion opening for guiding the insertion of a card into said loading section, the guide support including a pair of guide recesses formed along a pair of sidewalls of said loading section. It would have been obvious to those skilled in the art at the time the invention was made to provide a guide support provided in each of the loading sections and extending in a direction transverse to said insertion opening for guiding the insertion of memory chips into said loading sections, each said guide support including a pair of guide recesses formed along the pair of sidewalls of the loading section of the integrated circuit device as taught by Oliphant in the integrated circuit device of Klatt to allow for efficient and reliable insertion and removal of a component into the loading section of the integrated circuit device.

Regarding claim 2, the Klatt reference discloses a memory device adapted to be loaded in host equipment comprising a substantially rectangular main body unit 5 a first set of connection terminals 7 provided at one end of said main body unit to enable electrical connection between said main body unit and the host equipment, a plurality loading sections 21, 22 provided in said main body unit, each of said loading sections having an insertion opening along an edge of said main body unit transverse to said one end, a second set of connection terminals (necessarily provided for interfacing with inserted multimedia card MM) spaced from said insertion opening, and a pair of

sidewalls (walls directly adjacent loading sections 21, 22) disposed between said insertion opening and said second set of connection terminals, a plurality of substantially rectangular memory chips MM including a memory unit therein and a third set of connection terminals (contacts provided on the multimedia cards MM) for establishing electrical connection between said second set of connection terminals in said loading section and said memory unit, and a controller disposed in said main body unit for controlling the writing of information signals to and the readout of information signals from said plurality of integrated circuit chips loaded in said loading sections. Oliphant teaches that it is known to provide an integrated circuit device 40 adapted to be loaded in host equipment, a loading section provided in the main body unit 42, a guide support (area opposing guide recesses) provided in each of said loading sections and extending in a direction transverse to said insertion opening for guiding the insertion of said integrated circuit chips into said loading sections, each said guide support including a pair of guide recesses (notches along inner portion of sidewall of 42) formed along said pair of sidewalls (outer walls of 42) of said loading section. It would have been obvious to those skilled in the art at the time the invention was made to provide a guide support provided in each of the loading sections and extending in a direction transverse to said insertion opening for guiding the insertion of memory chips into said loading sections, each said guide support including a pair of guide recesses formed along the pair of sidewalls of the loading section of the integrated circuit device as taught by Oliphant in the integrated circuit device of Klatt to allow for efficient and

reliable insertion and removal of a component into the loading section of the integrated circuit device.

Regarding claim 3, it may be considered that the main body is approximately in the dimensions claimed.

Regarding claim 4, it appears that the memory unit is a flash memory. Furthermore, those skilled in the art at the time the invention was made would recognize that use of flash memory in integrated circuit chips is expedient in the art.

Regarding claim 5, the Klatt reference discloses an adapter device adapted to be loaded in host equipment comprising a substantially rectangular main body unit 5, a first set of connection terminals 7 provided at one end of said main body unit to enable electrical connection between said main body unit and the host equipment, a plurality loading sections 21, 22 provided in said main body unit, each of said loading sections having an insertion opening along an edge of said main body unit transverse to said one end, a second set of connection terminals (necessarily provided for interfacing with inserted multimedia card MM) spaced from said insertion opening, and a pair of sidewalls (walls directly adjacent loading sections 21, 22) disposed between said insertion opening and said second set of connection terminals, plurality of substantially rectangular integrated chips assembled in respective ones of said loading sections, each of said integrated circuit chips including a built-in integrated circuit unit forming a memory unit in electrical connection with said second set of connection terminals in said loading section, and a controller disposed in said main body unit for controlling the integrated circuit chips loaded in said loading sections. Oliphant teaches that it is

known to provide an integrated circuit device 40 adapted to be loaded in host equipment, a loading section provided in the main body unit 42, a guide support (area opposing guide recesses) provided in each of said loading sections and extending in a direction transverse to said insertion opening for guiding the insertion of said integrated circuit chips into said loading sections, each said guide support including a pair of guide recesses (notches along inner portion of sidewall of 42) formed along said pair of sidewalls (outer walls of 42) of said loading section. It would have been obvious to those skilled in the art at the time the invention was made to provide a guide support provided in each of the loading sections and extending in a direction transverse to said insertion opening for guiding the insertion of memory chips into said loading sections, each said guide support including a pair of guide recesses formed along the pair of sidewalls of the loading section of the integrated circuit device as taught by Oliphant in the integrated circuit device of Klatt to allow for efficient and reliable insertion and removal of a component into the loading section of the integrated circuit device.

Regarding claim 6, the Klatt reference discloses a substantially rectangular integrated circuit chip (MM card) adapted to be loaded in an adaptor device 5 for use in host equipment, said integrated circuit chip comprising a main body unit removably insertable into the adaptor device and having a pair of sidewalls, an integrated circuit unit disposed in said main body unit, a set of terminals provided at one end of said main body for establishing an electrical connection enabling information signals to be exchanged between said integrated circuit unit and the adaptor device. Oliphant discloses an integrated circuit device 40 adapted to be loaded in host equipment, a

loading section provided in the main body unit 42, a guide support (area opposing guide recesses) provided in each of said loading sections, each said guide support including a pair of protuberantly (protrusions along inner portion of sidewall of 42) formed guide sections formed along said pair of sidewalls (outer walls of 42) of said loading section. It would have been obvious to those skilled in the art at the time the invention was made to provide a guide support unit including a pair of protuberantly formed guide sections provided on said pair of sidewalls of said main body unit for guiding the insertion of said main body unit into a pair of guide recesses disposed along sidewalls of the adaptor device as taught by Oliphant in the device of Klatt to allow for efficient and reliable insertion and removal of a component into the loading section of the integrated circuit device.

Regarding claim 7, it appears that said integrated circuit chip is a flash memory. Furthermore, Furthermore, those skilled in the art at the time the invention was made would recognize that use of flash memory in integrated circuit chips is expedient in the art.

Regarding claim 8, it appears that the integrated circuit chip is a logic circuit unit.

Regarding claim 9, as noted above, the above mentioned combination as taught by the Klatt and Oliphant references disclose a substantially rectangular chip (MM card) adapted to be loaded in an adaptor device 5 for use in host equipment, said integrated circuit chip comprising a main body unit removably insertable into the adaptor device and having a pair of sidewalls, an integrated circuit unit disposed in said main body unit, a set of terminals provided at one end of said main body for establishing an electrical

connection enabling information signals to be exchanged between said integrated circuit unit and the adaptor device. Oliphant discloses an integrated circuit device 40 adapted to be loaded in host equipment, a loading section provided in the main body unit 42, a guide support (area opposing guide recesses) provided in each of said loading sections, each said guide support including a pair of protuberantly (protrusions along inner portion of sidewall of 42) formed guide sections formed along said pair of sidewalls (outer walls of 42) of said loading section. It would have been obvious to those skilled in the art at the time the invention was made to provide a guide support unit including a pair of protuberantly formed guide sections provided on said pair of sidewalls of said main body unit for guiding the insertion of said main body unit into a pair of guide recesses disposed along sidewalls of the adaptor device as taught by Oliphant in the device of Klatt to allow for efficient and reliable insertion and removal of a component into the loading section of the integrated circuit device. However, neither of these references teaches that the rectangular chip may be a dummy card. However, it is expedient in the art to provide dummy chip card for insertion into otherwise empty or nonused slots of adapters to provide environmental shielding from dust which may negatively impact the integrated circuit device or to provide electrical continuity or to provide voltage distribution. It would have been obvious to form a dummy card as configured above for placement into an otherwise empty slot to provide at least one of the advantages noted above.

Response to Arguments

3. Applicant's arguments have been fully considered but they are not persuasive but are moot in view of the new grounds for rejection.

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kaneda et al. (US 5,184,282).

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuong T. Vu whose telephone number is (571) 272-2111. The examiner can normally be reached on Mon. & Tues., 7:30 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on (571) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PTVu
Patent Examiner